Effects of suboxide layers on the electronic properties of Si(100)/SiO_2 interfaces: Atomistic multi-scale approach

Byung-Hyun Kim,[1,2] Gyubong Kim,[1,3,a)] Kihoon Park,[4] Mincheol Shin,[4,b)]
Yong-Chae Chung,[2] and Kwang-Ryeol Lee[1]
[1]*Center for Computational Science, Korea Institute of Science and Technology, Seoul 136-791, South Korea*
[2]*Department of Materials Science and Engineering, Hanyang University, Seoul 133-791, South Korea*
[3]*Division of Material Science, Korea Basic Science Institute, Daejeon 305-806, South Korea*
[4]*Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, South Korea*

(Received 11 December 2012; accepted 28 January 2013; published online 15 February 2013)

A multi-scale approach connecting the atomistic process simulations to the device-level simulations has been applied to the Si(100)/SiO_2 interface system. The oxidation of Si(100) surface was simulated by the atomic level molecular dynamics, the electronic structure of the resultant Si/suboxide/SiO_2 interface was then obtained by the first-principles calculations, and finally, the leakage currents through the SiO_2 gate dielectric were evaluated, with the obtained interface model, by the non-equilibrium Green's function method. We have found that the suboxide layers play a significant role for the electronic properties of the interface system and hence the leakage currents through the gate dielectric. © *2013 American Institute of Physics*.
[http://dx.doi.org/10.1063/1.4791706]

I. INTRODUCTION

Recent progress in semiconductor devices, represented by the Moore's law, has realized the oxide thickness approaching 1 nm in metal oxide semiconductor field effect transistors (MOSFETs) that conventionally use the SiO_2 dielectric.[1] The electronic properties of such a thin gate stack are significantly affected by the suboxide layer of only a few angstroms in thickness that is inevitably formed during the dielectric layer growth. Understanding the detailed interface morphology of Si/SiO_2 including the suboxide layer can be an essential issue to determine the device performance and reliability.[2,3] Several experimental observations have elucidated the presence of the suboxide layer showing substoichiometry at the interface between Si/SiO_2 with a thickness ranging from 0.5 to 1 nm.[4–6] However, most of the theoretical investigations on the Si/SiO_2 interface system disregarded the presence of the suboxide layer because of its complexity. For example, Yamasaki *et al.*[7] performed the *ab initio* molecular dynamics (MD) calculation for the electronic structures of various crystalline phases of the SiO_2 on Si(001). Ribeiro *et al.*[8] employed the density functional theory (DFT) calculation to calculate the band gaps and band offsets of the SiO_2/Si interface model. Although their results could reveal the atomistic understanding of the electronic structure of SiO_2/Si interface, the interface of SiO_2/Si without considering the suboxide layer is not realistic.

In this work, we address the effect of the suboxide layer on the electronic properties of the Si/SiO_2 interface system with a multi-scale approach involving the MD simulations, the first-principles calculations, and the non-equilibrium Green's function (NEGF) method. It is demonstrated that the suboxide layer at the Si/SiO_2 interface plays a substantial role for the electronic properties of the gate stack.

II. COMPUTATIONAL METHODS

The overall procedure of our multi-scale approach is as follows: The MD simulations were performed to identify the atomic structures of Si(100)/suboxide/SiO_2 interfaces. The suboxide structures were then modeled based on the result of the MD simulations to obtain the band gap profiles with the DFT calculations. Finally, the obtained band gap profiles were used to calculate the leakage currents of the gate stack by using the NEGF method.

A. MD simulations

We carried out MD simulations of dry oxidation on a single crystal Si(100) surface using the reactive force field (ReaxFF) proposed by van Duin *et al.*[9] The ReaxFF for Si-O system used in this study was rigorously benchmarked in the previous work.[10] The size of the Si(100) substrate was $15.47 \times 15.47 \times 47.86$ Å^3. Periodic boundary conditions were applied in both the x and y directions. The atomic positions of the bottommost layer were fixed to simulate a thick substrate. The oxidation temperature was set to 1073 K to mimic a typical thermal dry oxidation. The dry oxidation process simulation was initiated with inserting 400 O_2 molecules in the simulation box after the Si(100) substrate was relaxed for 50 ps. After the dry oxidation process of 100 ps, the O_2 molecules, which were not reacted with the silicon atoms in the substrate, were removed in the system. Then, the dry oxidation process was again performed with inserting 400 O_2 molecules in the system for 100 ps. Finally, the system was fully relaxed for 100 ps at 1073 K and cooled to 10 K with steps of approximately 4 K per 1 ps. The final system was used to analyze the atomic configuration of

a)Email: kgb531@kbsi.re.kr.
b)Email: mshin@kaist.ac.kr.

$Si(100)/SiO_x/SiO_2$. "Large-scale Atomic/Molecular Massively Parallelized Simulator" (LAMMPS) code[11] integrated with ReaxFF was used for the MD simulations in this work.

B. DFT calculations

The DFT calculations were performed by using the Vienna ab-initio simulation package.[12] The projector augmented wave pseudopotentials[13] were used, and the electron exchange-correlation was treated within the generalized gradient approximation (GGA) of Perdew-Burke-Ernzerhof type.[14] The cutoff energy for the planewave-basis expansion was chosen to be 212 eV, and the atomic relaxation for all modeled interface structures (see Fig. 2) was carried out until Helmann-Feynman forces acting on atoms are less than 0.02 eV/Å (only the bottommost Si atoms passivated with hydrogen atoms are fixed to maintain their bulk interatomic distances). The supercell method is employed with the distance between slabs in the supercells set to about 20 Å.

C. NEGF method

The gate leakage current was calculated using an in-house code, which is based on the 1-D NEGF approach. The retarded Green's function expressed in the following equation is firstly calculated:

$$G(E_x) = [E_x I - H - \Sigma_1 - \Sigma_2]^{-1}, \quad (1)$$

where H is the device Hamiltonian and $\Sigma_{1,2}$ are the substrate and gate electrode self-energies, respectively. In this work, the parabolic effective mass Hamiltonian was used to describe electrons in the Si conduction band. Once the Green's function is calculated, the electron carrier density can be readily obtained using the following expression:

$$n(x) = \int \frac{dE_x}{2\pi}[A_1(E_x)F_1(E_x - \mu_1) + A_2(E_x)F_2(E_x - \mu_2)], \quad (2)$$

where

$$F_{1,2}(E_x - \mu_{1,2}) = \sum_{k_y,k_z} f_{1,2}\left(E_x + \frac{\hbar^2 k_y^2}{2m_y^*} + \frac{\hbar^2 k_z^2}{2m_z^*} - \mu_{1,2}\right) = \frac{\sqrt{m_y^* m_z^*} k_B T}{\pi\hbar^2} \ln\left[1 + \exp\left(\frac{\mu_{1,2} - E_x}{k_B T}\right)\right]. \quad (3)$$

The spectral functions, $A_{1,2}$, in Eq. (2) are represented as

$$A_{1,2}(E_x) = G\Gamma_{1,2}G^\dagger, \quad (4)$$

where the broadening matrices are given by

$$\Gamma_{1,2} = i(\Sigma_{1,2} - \Sigma_{1,2}{}^\dagger). \quad (5)$$

To appropriately take into account the effects of the quasi-bound states (QBSs), we adopted the so-called "optical potential" method.[15] The role of the optical potential, which has a magnitude of few meV, is to broaden the energy levels sufficiently so that the electron density and transmission can be computed. By iteratively solving the electron density distribution calculated using the above NEGF equation, and the potential profile calculated using the Poisson equation, we obtain a self-consistent solution. The resultant potential profile is used to calculate the transmission probability expressed in terms of the Green's function as

$$T(E_x) = Tr[\Gamma_2 G \Gamma_1 G^\dagger]. \quad (6)$$

The gate leakage current density is finally calculated using the equation

$$J = \frac{2q\sqrt{m_y^* m_z^*} k_B T}{(2\pi)^2 \hbar^3} \int dE_x T(E_x) \ln\left[\frac{1 + \exp\left((\mu_1 - E_x)/k_B T\right)}{1 + \exp\left((\mu_2 - E_x)/k_B T\right)}\right]. \quad (7)$$

III. RESULTS AND DISCUSSION

A. Oxidation process simulation

Figure 1 shows the atomic configuration of $Si(100)/SiO_x/SiO_2$ colored by the Mülliken charge after the oxidation process and the corresponding radial distribution functions (RDFs). The RDF of SiO_2 layer (Fig. 1(d)) was found to be comparable with that of amorphous silica generated by melting and quenching processes,[16] which indicates that the SiO_2 layer was fully amorphized during the oxidation process. Si atoms in the SiO_2 layer have approximately +1.4 e and O atoms approximately −0.8 e; these values are similar to those of the previous calculation with α-quartz.[9] The atomic ratio of oxygen to silicon in the SiO_2 layer was 1.90. However, a non-stoichiometric suboxide layer with a thickness of approximately 6 Å was observed between the SiO_2 layer and the crystalline Si region, which agrees well with the previous experimental observations.[4–6] From the RDF analysis, it was observed that the structure of SiO_x (Fig. 1(c)) is an intermediate state between crystalline Si and amorphous silica since the positions of the first peak of Si-Si bonds and Si-O bonds correspond with those for crystalline Si (Fig. 1(b)) and amorphous silica (Fig. 1(d)), respectively. The atomic composition of silicon to oxygen in the suboxide layer is found to be approaximately 2.19.

B. Electronic structure of Si/SiO_2 interface

Based on the atomic composition of the suboxide layer obtained from the MD simulations, we calculated the band gap profiles of the $Si(100)/suboxide/SiO_2$ structure with the DFT calculations. The model $Si(100)/(Si_2O)_x$/α-quartz interface system is considered, where Si_2O is the atomic composition that best mimics the suboxide layers obtained from the MD simulation (see Fig. 1) and the subscribt x denotes the number of the Si_2O layers. Here the α-quartz represents the ideal SiO_2 dielectric as introduced in the literatures.[7,17] The Si_2O layers are formed sequentially increasing O adatoms under the α-quartz as shown in Fig. 2.

We examined the band gap profiles along the z-axis (perpenticular to the interface plane) of $Si(100)/(Si_2O)_x$/α-quartz up to $x = 4$, because $(Si_2O)_4$ gives the thickness of about 6 Å, which is closest to the thickness of the suboxide layers as observed in the MD calculation (see Fig. 1). The

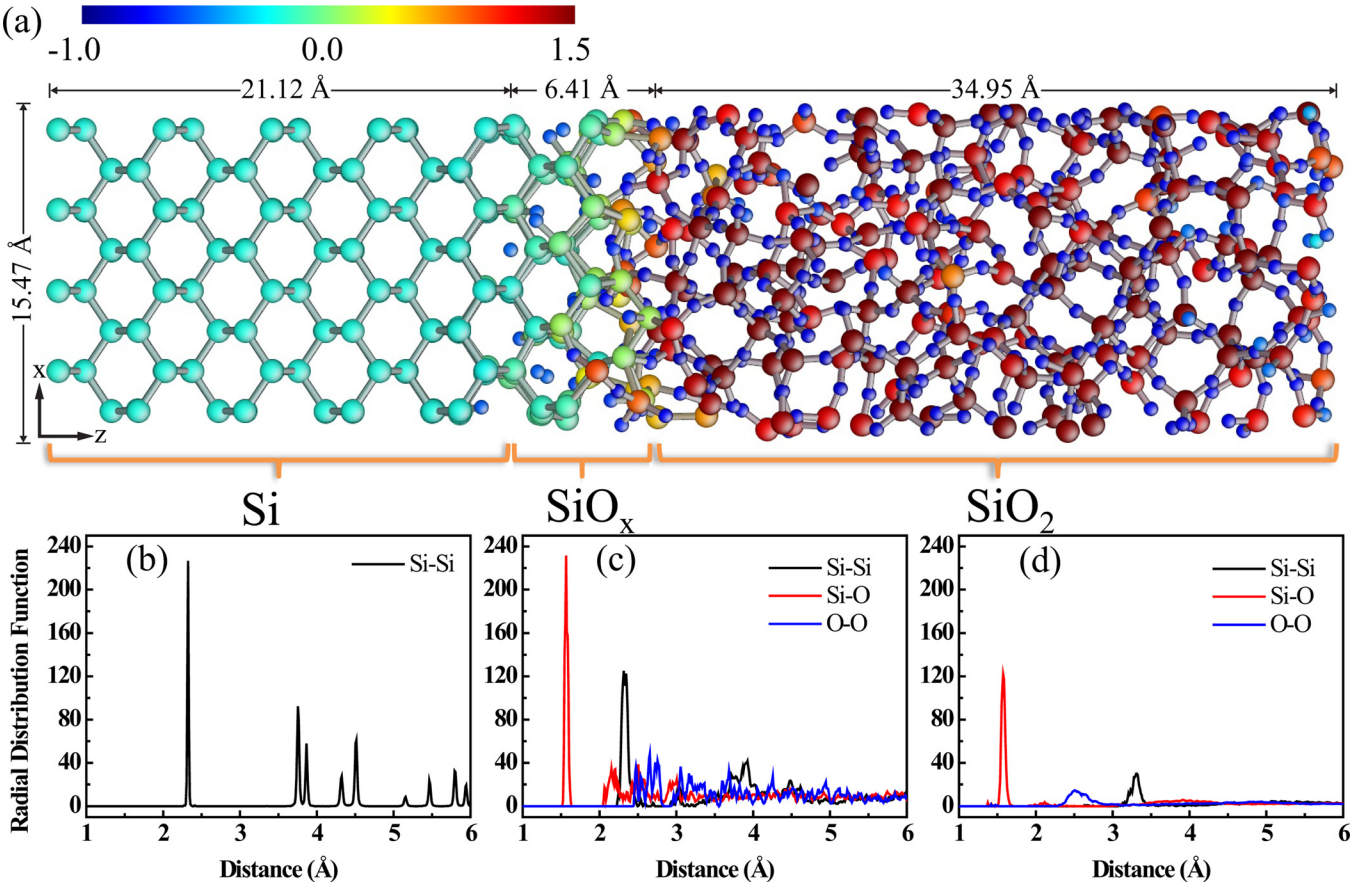

FIG. 1. (a) The atomic configuration of Si(100)/SiO_x/SiO_2 colored by the Mülliken charge as in the scale bar after the MD simulation of the dry oxidation process. The corresponding radial distribution functions of (b) crystalline Si layer (c) SiO_x suboxide layer, and (d) amorphous SiO_2 layer.

conduction band minima (CBM) and the valence band maxima (VBM) were determined by the energy values at which the local density of states of Si atoms becomes less than 0.001 (see Fig. 2 for the details about the CBM and the VBM).

For the sharp interface of the Si(100)/α-quartz structure, i.e., the interface without the suboxide layers, there exists the band-gap transition region of ∼5 Å-thick across the interface.[7,17] We observed that including Si_2O layers results in notably different band gap profiles from those of the

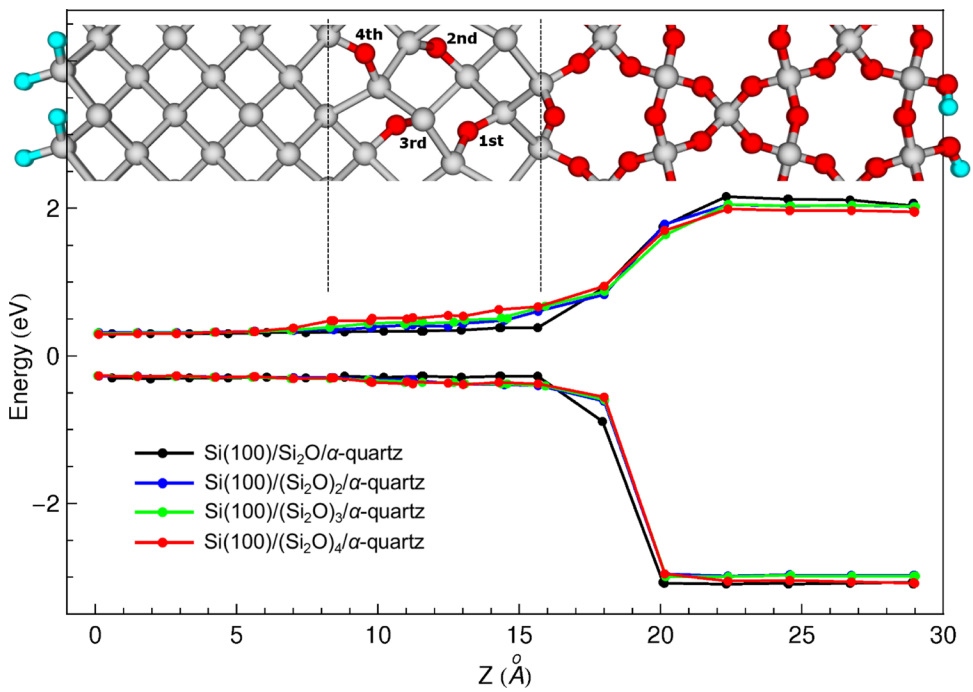

FIG. 2. Optimized configuration of the modeled Si(100)/$(Si_2O)_4$/α-quartz system and the band gap profiles of Si(100)/$(Si_2O)_x$/α-quartz along z-axis. The white, red, and cyan balls denote the Si, O, and H atoms, respectively. We added O atoms sequentially to increase the number of the Si_2O layers under the α-quartz (see the sequence of O adatoms in the Si_2O region). CBM and VBM are determined by the energy values where the density of states (states/eV) decreases to less than 0.001. Note that increasing the number of Si_2O layers elevates their CBM in energy.

sharp-interfaced Si(100)/α-quartz system. As shown in Fig. 2, with only one layer inserted, the bandgap transition behavior is almost the same as that of the Si(100)/α-quartz system (see the transition region between about 16 and 21 Å).[7,17] As the Si_2O layers become thicker, however, its CBM are gradually elevated in energy, whereas its VBM are slightly shifted down. Eventually, in the 6 Å thick Si_2O region, a step of 0.2 eV high is formed as shown by the four layer ($x = 4$) case in Fig. 2. It is also worth to note that, as the conventional DFT calculations are known to underestimate the band offsets when compared to more elaborated calculation methods such as GW or hybrid functional calculations,[18,19] the presented offset of CB, 0.2 eV, at the $Si/(Si_2O)_4$ interface can be regarded as the lower limit of the band offset that can occur at this interface.

C. Gate leakage current of Si/SiO_2 MOS system

In a Si/SiO_2 MOS system, it is a common practice to model the CB profile as abruptly changing at the interface. But as illustrated above, the CB profile is in fact quite different from being abrupt, due to the presence of both the 6 Å thick suboxide layer and the 5 Å thick transition region in the SiO_2 side. This will affect the performance of the n-type device as discussed in the followings.

The gate leakage current in n-type MOSFETs with the SiO_2 gate dielectric was evaluated using the above-obtained $Si(100)/(Si_2O)_x/SiO_2$ CBM profile. The model device for the leakage current calculations consists of an n^+-poly-Si gate, SiO_2 dielectric layer and a p-Si substrate. Figure 3 shows the schematic diagram of the simulated device structure. We assume that the channel is long enough so that there is no influence of the source and drain contacts or biases on the potential obtained using the formulas above. The doping levels in the gate electrode and substrate are $N_D = 2 \times 10^{19}\,cm^{-3}$ and $N_A = 5 \times 10^{17}\,cm^{-3}$, respectively, and are assumed to be uniformly doped and completely ionized. All the six valleys of the Si conduction band are considered in our calculations. The effective masses for the two-fold degenerate valleys and the four-fold degenerate valleys of the silicon substrate are assumed to be $m_l = 0.916m_0$ and $m_t = 0.191m_0$, respectively. For the oxide layer, the isotropic effective mass of $m_{ox} = 0.4m_0$ is used. Since the conduction band offset of the $Si\text{-}SiO_2$ layer is 3.1 eV, we scaled the

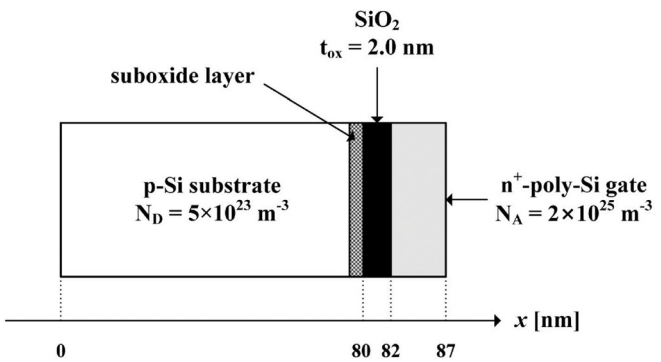

FIG. 3. Schematic diagram of the simulated device structure is plotted. The *x*-direction is the transport direction.

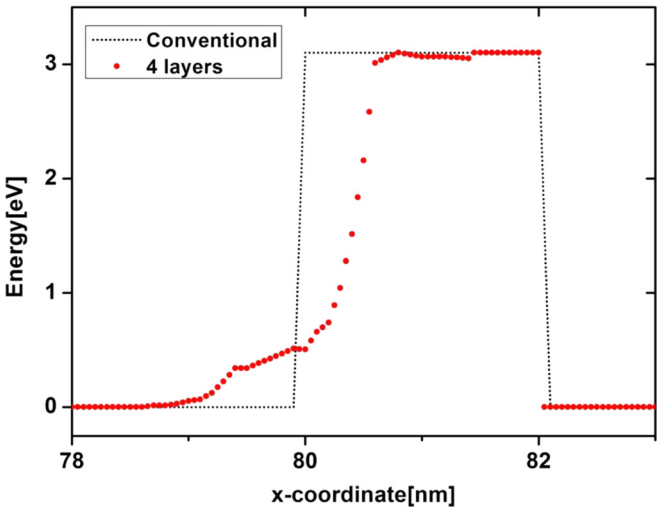

FIG. 4. CB profiles for the conventional model and the 4-layer-suboxide model are plotted together for comparison. Notice the presence of both the 6 Å thick suboxide layer and the 5 Å thick transition region in the SiO_2 side.

CBM of the $Si/(Si_2O)_x/SiO_2$ accordingly. The CB profiles for the conventional model and the 4-layer-suboxide model are plotted together for comparison in Fig. 4.

Figure 5 shows the calculated gate-leakage current density J_G through a 2 nm thick SiO_2 gate dielectric. The effects of the suboxide layers on J_G can be clearly seen in the figure. If we compare the 4-suboxide-layer case with the case of the conventional abrupt interface case, J_G of the former becomes about one order lower than the latter in the low gate bias region while there is a crossover of J_G in the high gate bias region. As discussed above, the thicker the Si_2O slab becomes, the higher its CBM become elevated with respect to the Si substrate. This leads to a decrease in the leakage current under low gate biases, because it becomes more difficult for electrons to tunnel through the thus-thickened barrier at the low energy range. On the other hand, under high gate

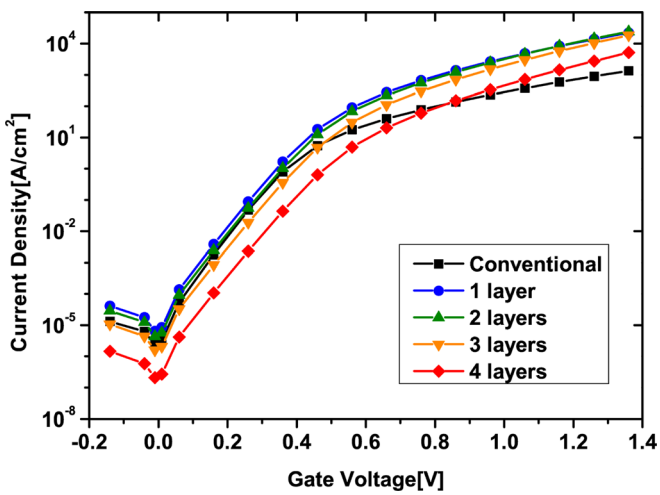

FIG. 5. Gate leakage current for the conventional Si/SiO_2 abrupt interface model with no suboxide layer and the model proposed here are plotted together. The curves for 1, 2, 3, 4 layers are the number of the suboxide Si_2O layers. Under low gate bias, the leakage current is suppressed due to the suboxide layer. Under high gate bias, the current gets larger than the conventional case due to the tunneling electrons in the high energy region.

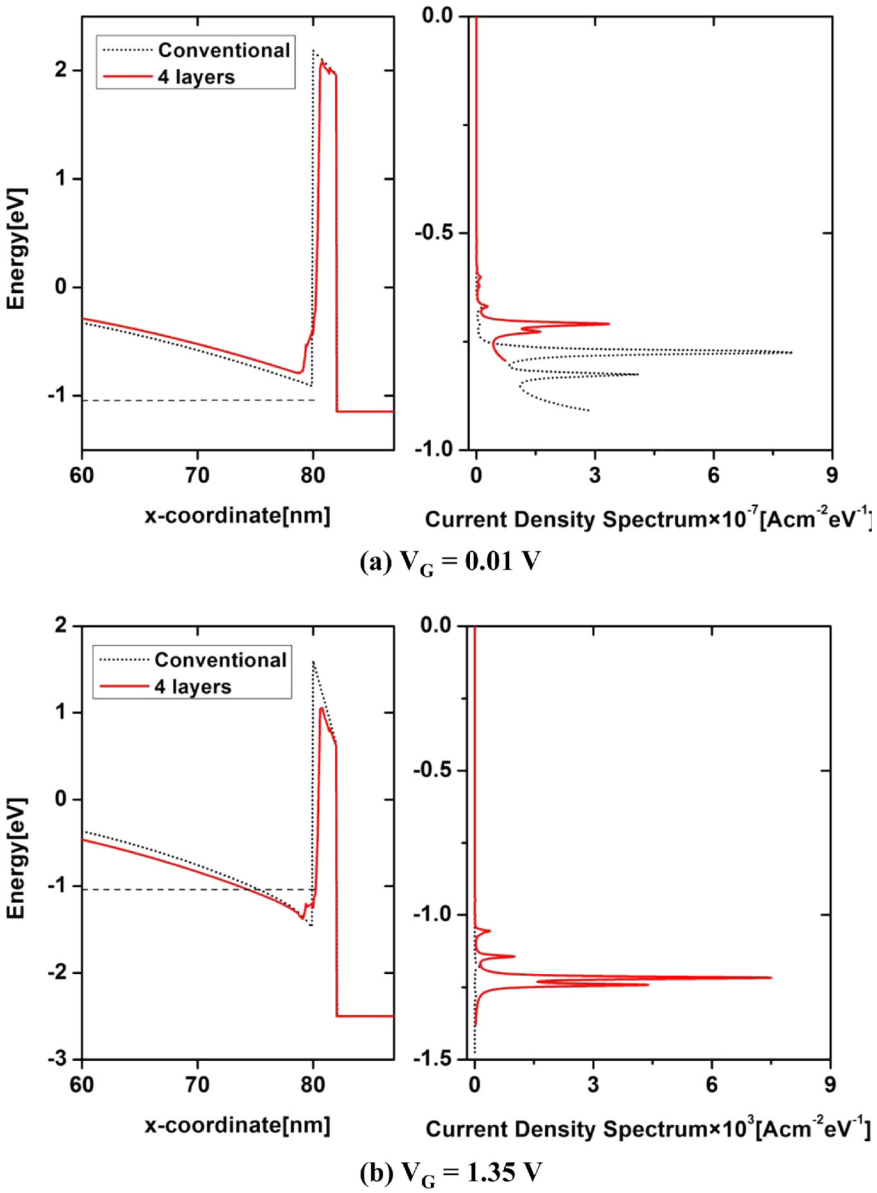

FIG. 6. Potential profiles and current density spectrums are plotted side-by-side for (a) a low gate bias ($V_G = 0.01$ V) and (b) a high gate bias ($V_G = 1.35$ V). The dashed lines represent the substrate's Fermi level, $E_F = -1.05$ V.

biases, tunneling through the thinner barrier at the high energy range (due to the 5 Å thick transition region in the SiO_2 side) also contributes to the leakage currents, resulting in the cross-over. These points are illustrated in Fig. 6, which shows the potential profiles and current density spectrums side-by-side for (a) a low gate bias ($V_G = 0.01$ V) and (b) a high gate bias ($V_G = 1.35$ V). At a low gate bias, we can see that, compared to the conventional model, the 4 layer model has a thicker tunneling barrier near the Fermi level. However, at a high gate bias, the 4 layer model has a thinner tunneling barrier than the conventional abrupt interface model even below the Fermi level, resulting in a much higher current density.

In Fig. 7, the gate tunneling current density at a fixed low gate bias ($V_G = 0.01$ V) as a function of SiO_2 thickness is plotted. Compared to the conventional abrupt interface model, the impact of our 4-layer-suboxide layer model lies in the "gain" of the SiO_2 thickness as much as 2.5 Å. In other words, the SiO_2 gate dielectric can be 2.5 Å thinner than that suggested by the conventional abrupt interface model and

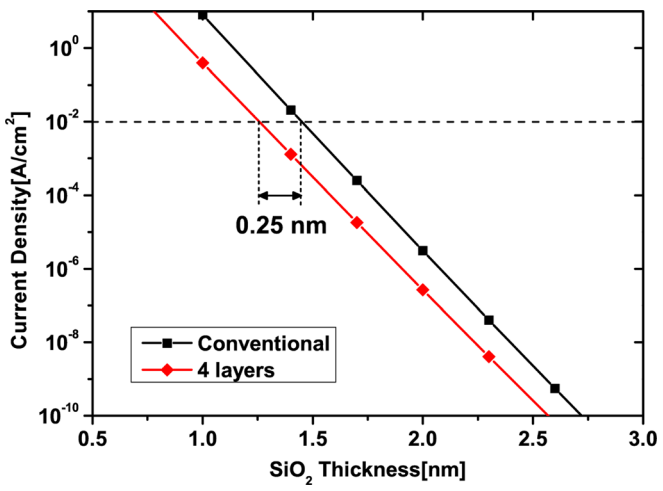

FIG. 7. Gate leakage current density at a fixed low gate bias ($V_G = 0.01$ V) as a function of SiO_2 thickness for the conventional Si/SiO_2 abrupt interface model and the 4-layer-suboxide model.

still maintain the same leakage current density. Considering that the state-of-the-art devices are entering the sub-10 Å dielectric thickness regime,[20] this difference is not ignorable at all.

IV. CONCLUSIONS

In summary, we investigated the electronic properties of the Si(100)/suboxide/SiO_2 interface structure with a multi-scale approach, involving the atomic level MD simulation, the first principles calculation and the NEGF method, which encompasses the process simulations and the device-level simulations. The massive MD simulations of planar Si(100) oxidation revealed that the suboxide layer is formed with the atomic composition close to Si_2O. Based on this observation, we modeled the Si(100)/$(Si_2O)_x$/SiO_2 interface and calculated the band gap profiles across the interfaces with the use of the DFT calculations, which indicated that including the Si_2O layers results in notably different band gap profiles from those of the Si(100)/SiO_2 system without the suboxide layers. The device-level simulations using the NEGF method demonstrated that the band structures as modified by the Si_2O layers significantly affect the leakage current through the SiO_2 gate dielectric. Our MD-DFT-NEGF multi-scale approach suggests that, in achieving the same leakage current level at low gate biases, the SiO_2 gate dielectric can be 2.5 Å thinner than that suggested by the conventional simplistic approach.

ACKNOWLEDGMENTS

The present research was financially supported by the Converging Research Center Program through the Ministry of Education, Science and Technology (2012K001314, 2012K001315). The authors gratefully acknowledge SR11000 supercomputing resources from the Center for Computational Materials Science of the Institute for Materials Research, Tohoku University.

[1]D. A. Buchanan, IBM J. Res. Dev. **43**, 245 (1999).
[2]D. A. Muller, T. Sorsch, S. Mocci, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, Nature (London) **399**, 758 (1999).
[3]S. Iwata and A. Ishizaka, J. Appl. Phys. **79**, 6653 (1996).
[4]A. R. Chowdhuri, D.-U. Jin, J. Rosado, and C. G. Takoudis, Phys. Rev. B **67**, 245305 (2003).
[5]J. H. Oh, H. W. Yeom, Y. Hagimoto, K. Ono, M. Oshima, N. Hirashita, M. Nywa, A. Toriumi, and A. Kakizaki, Phys. Rev. B **63**, 205310 (2001).
[6]H. Ono, T. Ikarashi, K. Ando, and T. Kitano, J. Appl. Phys. **84**, 6064 (1998).
[7]T. Yamasaki, C. Kaneta, T. Uchiyama, T. Uda, and K. Terakura, Phys. Rev. B **63**, 115314 (2001).
[8]M. Ribeiro, L. R. C. Fonseca, and L. G. Ferreira, Phys. Rev. B **79**, 241312(R) (2009).
[9]A. C. T. v. Duin, A. Strachan, S. Stewman, Q. Zhang, X. Xu, and W. A. Goddard III, J. Phys. Chem. A **107**, 3803 (2003).
[10]M. A. Pamungkas, M. Joe, B.-H. Kim, and K.-R. Lee, J. Appl. Phys. **110**, 053513 (2011).
[11]S. Plimpton, J. Comp. Phys. **117**, 1 (1995).
[12]G. Kresse and J. Furthmüller, Phys. Rev. B **54**, 11169 (1996).
[13]G. Kresse and D. Joubert, Phys. Rev. B **59**, 1758 (1999).
[14]J. P. Perdew, K. Burke, and M. Ernzerhof, Phys. Rev. Lett. **77**, 3865 (1996).
[15]R. Lake, G. Klimeck, R. C. Bowen, and D. Jovanovic, J. Appl. Phys. **81**, 7845 (1997).
[16]J. C. Fogarty, H. M. Aktulga, A. Y. Grama, A. C. T. v. Duin, and S. A. Pandit, J. Chem. Phys. **132**, 174704 (2010).
[17]M. Shin, Y. Park, K.-J. Kong, and H. Chang, Appl. Phys. Lett. **98**, 173501 (2011).
[18]A. Alkauskas, P. Broqvist, F. Devynck, and A. Pasquarello, Phys. Rev. Lett. **101**, 106802 (2008).
[19]R. Shaltaf, G.-M. Rignanese, X. Gonze, F. Giustino, and A. Pasquarello, Phys. Rev. Lett. **100**, 186401 (2008).
[20]A. Chin, W. B. Chen, B. S. Shie, K. C. Hsu, P. C. Chen, C. H. Cheng, C. C. Chi, Y. H. Wu, K. S. Chaing-Liao, S. J. Wang, C. H. Kuan, and F. S. Yeh, 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (2010), p. 836.